CHARGE-COUPLED SCANNED IR IMAGING SENSORS

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A program for making two-dimensional IR-CCD imaging arrays is well under way. The design is discussed in detail. Plans for making quantitative infrared measurements are also discussed, and initial experiments are described.

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PREFACE

This Technical Report was prepared by RCA Laboratories, Princeton, New Jersey, under Contract No. F19628-73-C-0282 and ARPA Order No. 2444. It describes work performed from 1 May 1975 to 30 October 1975, in the Integrated Circuit Technology Center. E. S Kohn was the Principal Investigator; the Project Supervisor was K. H. Zaininger. Other members of the Technical Staff who participated in the research were: J. E. Carnes, W. F. Kosonocky, and P. Levine of RCA Laboratories. R. D. Larrabee of RCA Advanced Technology Laboratories, Camden, New Jersey planned and performed infrared measurements.

The manuscript of this report was submitted by the authors on 14 November 1975. Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

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I. INTRODUCTION

The ultimate goal of this work is the fabrication of a two-dimensional infrared imager. Our previous work with the 64 x 1 line array has proven the feasibility of the Schottky-barrier detector silicon/CCD system, and has, in the vidicon mode, demonstrated a uniformity approaching that needed for thermal imaging. In the present work, the two-dimensional imager is being designed and fabricated. The first arrays will again have palladium-silicide on p-silicon as the detector system, but subsequent arrays will be made with platinum-silicide for deeper IR response. A line array is also included on the chip to provide additional features. The considerations that have gone into the design are discussed below. Quantitative infrared measurements have already begun and have yielded good agreement with previous measurements on the absolute quantum efficiency of PdSi:p-Si detectors. Additional quantitative infrared measurements have been planned and are discussed below in some detail.

II. DESIGN OF THE TWO-DIMENSIONAL IR-CCD

The 64 x 1 line array was a 3-phase device, made with a single level of metallization with gaps. The channel was 5 mils wide, and an additional 10 mils of width was used for the diffused clock busses. The detectors were long in the direction perpendicular to the line, and the charging circuit consumed additional width. Width is cheap in a line array, and no effort was made to conserve it. The design considerations for the two-dimensional (2D) array are quite different. Designs involving transfer gaps are considered undesirable because of experience obtained during the past few years, our good experience with the IR-CCD line array notwithstanding. Sealed channel (gapless) structures, in general, give better transfer efficiency, better device stability, and less sensitivity to mask tolerances, the latter fact resulting in better yields. A single level of metal also permits little design flexibility, requiring diffused crossunders and their associated contact holes for any but the simplest structures. This approach wastes area. For these reasons, the 2D array is being made with overlapping gates. The gates will consist of two levels of polysilicon strapped by aluminum, a system used successfully on other projects at the RCA Laboratories. The levels of polysilicon are individually oxidized immediately after definition. Contact holes are made in both levels of polysilicon and in the gate oxide all in one step, and palladium-silicide is formed in all contact holes in one step. Barriers are thus formed where the original substrate is contacted. Ohmic contacts are formed in the holes at the two levels of polysilicon and at source-drain diffusions in the substrate. An aluminum metallization and definition step straps the conductors together and completes the device.

The major problem in the design of the 2D IR-CCD array is the efficient use of area. Since it is the advantage of frame storage that makes Schottky-barrier area arrays competitive with more efficient line arrays, it is essential to have a reasonable fraction of the array area used for detection. The charge-coupled shift registers necessarily occupy a good part of the area. Thus, the structure must be such as to minimize the area budgeted for compliance with design rules and processing tolerances. This was a strong reason for selection of the double-polysilicon-gate system.

An outline of the 2D array is shown in Fig. 1. It is an "interline" system, with all detectors transferring their signals into the shift register at once in response to a pulse on the transfer gate. The column registers are then clocked down one bit, bringing the charge packets from the bottom row of detectors into the horizontal register. The latter is then clocked out, producing one horizontal line on the display. The column registers are subsequently clocked down one bit for each row of detectors. When the entire array has been read out in this manner, the transfer gate is pulsed again, loading the next frame. A natural consequence of this layout (as seen in Fig. 1) is that the detectors are spaced more closely in the vertical direction than in the horizontal direction. The channel width must be minimized for this reason as well as area utilization. Wiring the clock gates for two-phase operation would simplify the gate bussing but would limit the well capacity. It would also create a conflict between the substrate doping required for efficient two-phase operation and the substrate doping required for the

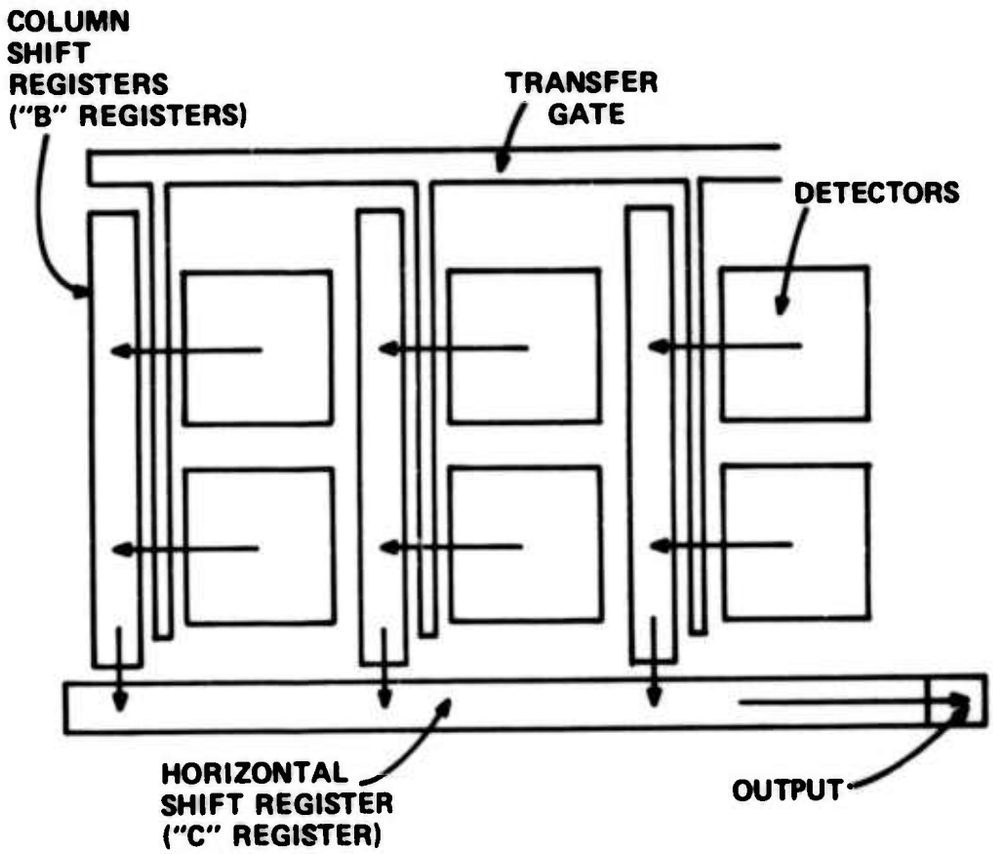

Fig. 1. Interline transfer scheme for the two-dimensional array.

detectors. We must, therefore, bus out the clock gates for four-phase operation. Connecting the gates horizontally across the chip between the detectors wastes detector area. We have worked out designs with the gates bussed vertically for each column, on each side of the channel, and while such a design is a big improvement, the columns are still wider than we would like. The design we adopted is unique and is outlined in Fig. 2. A scale drawing is shown in Fig. 3. The overlapping, four-phase gates for each column are defined and strapped separately, making use of the two layers of silicon and one of aluminum. The channel and transfer gate, with overlapping clock busses, are about 3 mils wide. The detector holes are about 2.5 mils square, and are spaced 3.2

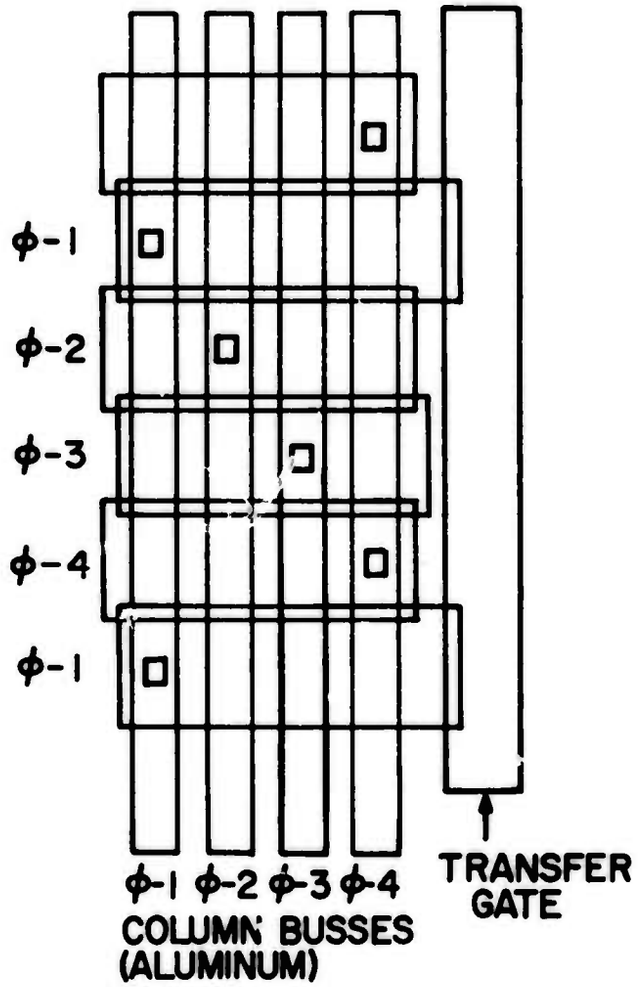

Fig. 2. Connection of gates in a typical column. The column straps are themselves bussed across at the top. The transfer gate and the phase 2 and 4 gates are first-level polysilicon while the phase 1 and 3 are second-level polysilicon.

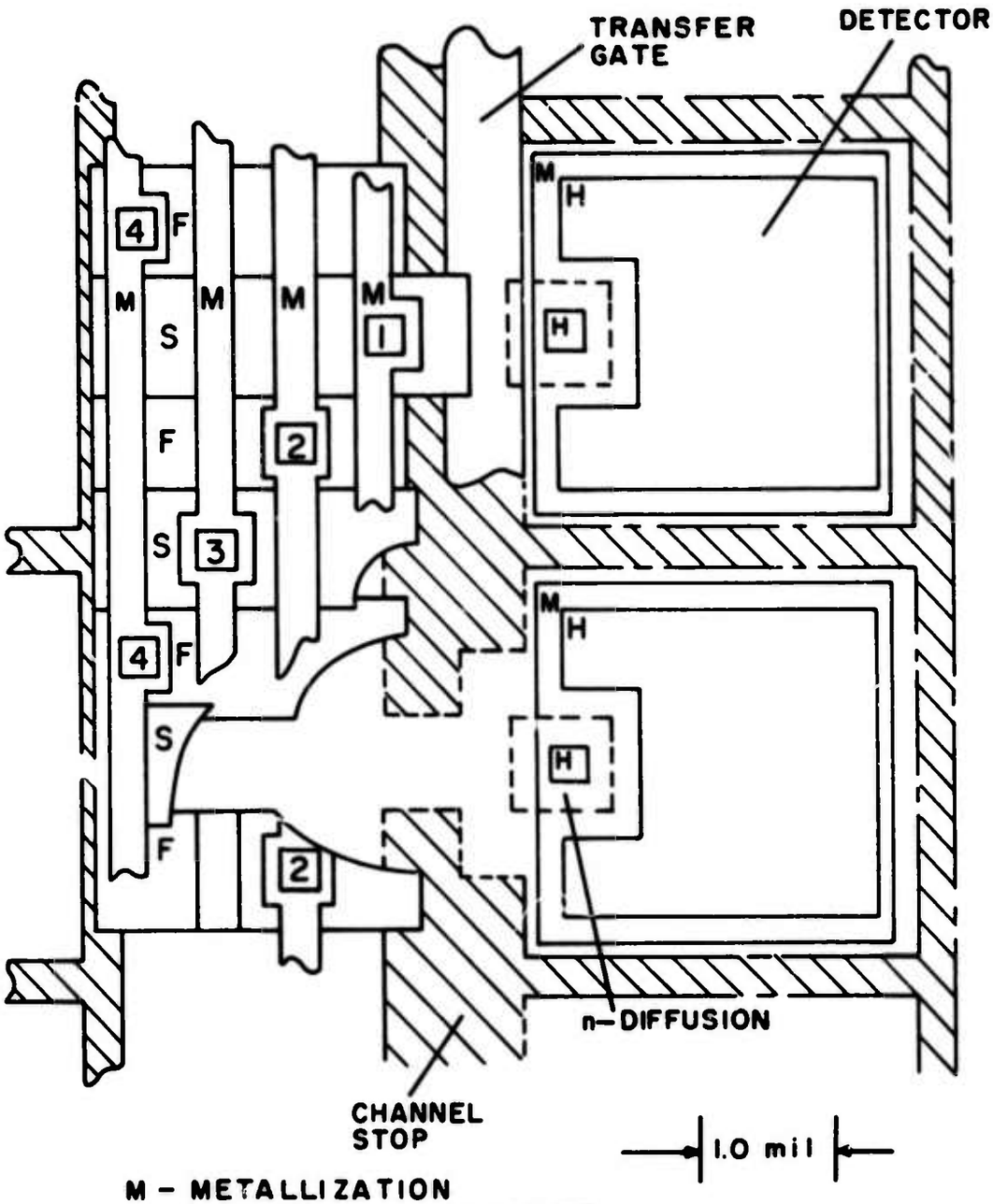

Fig. 3. Scale drawing of vertical shift register adjacent to two detectors. The source-drain diffusions are shown as dashed lines, while the channel-stop diffusions are crosshatched. Hidden lines are omitted for clarity, but are shown in cutaway section. The solid polygons are labeled according to the key in the figure.

mils apart vertically and 6.4 mils apart horizontally. Twenty-five percent of the repeated area is used for infrared detection. The 3.2-mil vertical bit length corresponds to gates 0.8 mil long in the direction of transfer. While these gates are relatively long, they present no problem at clock rates of a few hundred kHz. We could get faster performance with 8 gates per detector, each 0.4 mil long, but t.. ..e would not be enough room for good contact holes when strapped as in Fig. 2.

Detailed drawings of two other parts of the array are shown in Figs. 4 and 5. Figure 4 illustrates how charge is transferred from the column ("B") registers to the output ("C") register. The last two gates of the "B" registers are bussed separately as shown. Figure 5 illustrates the output section. The "C"-register channel terminates in the U-shaped, floating diffusion and the drain diffusion. Connected to the floating diffusion is the gate of an MOS transistor fabricated at the same time as the array.

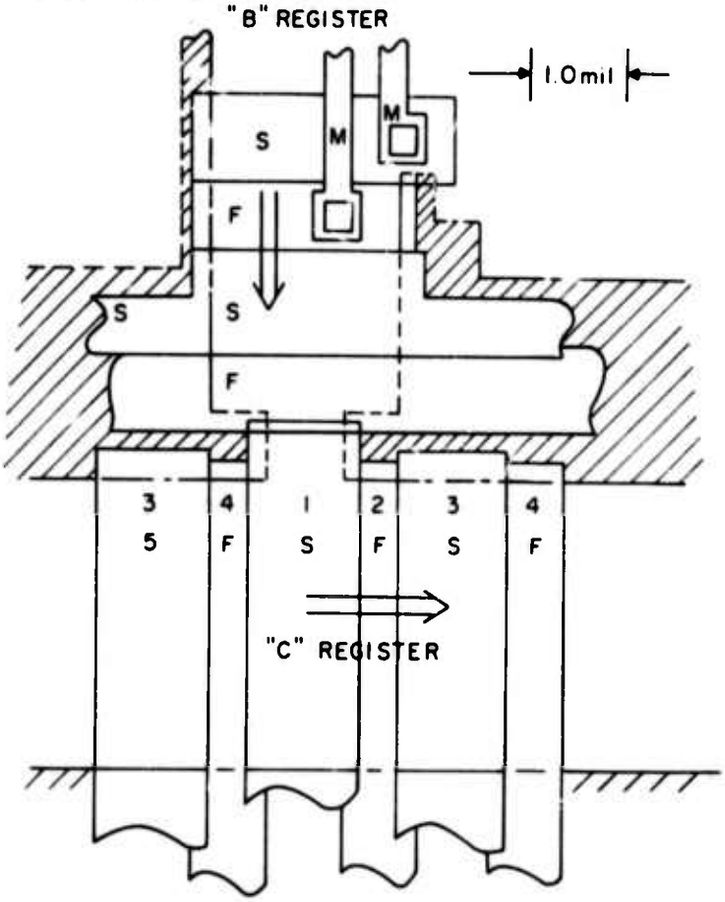

Fig. 4. Scale drawing of "B" to "C" transfer structure. Hidden lines are deleted for clarity, except for the channel-stop diffusion which is crosshatched where not hidden. The solid polygons are identified as in Fig. 3. Arrows indicate the direction of charge flow.

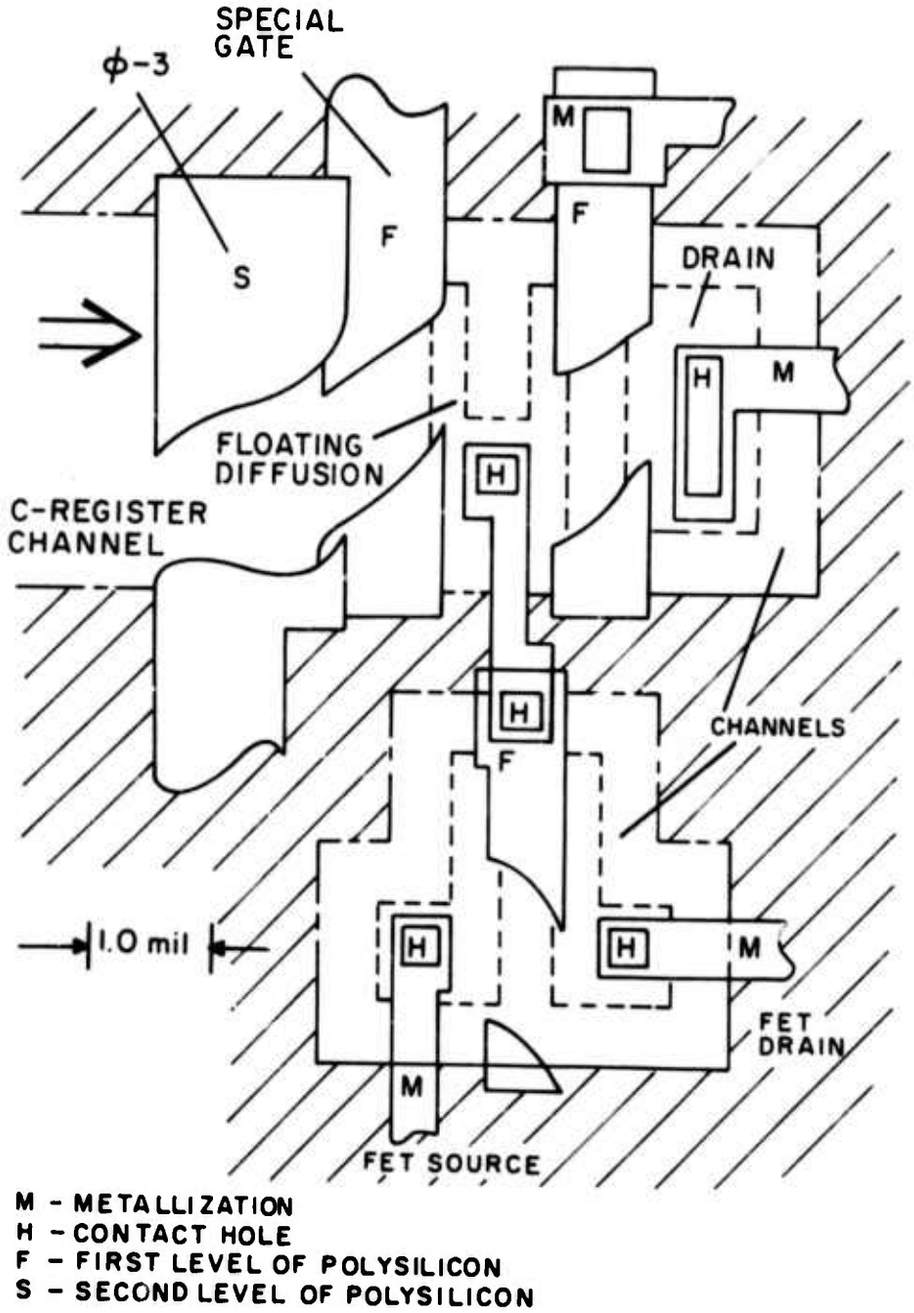

Fig. 5. Scale drawing of the output section. The channel-stop diffusion is crosshatched, and all hidden lines are deleted.

There were several reasons for not including a charging gate and charging diffusion in this 2D design. This structure would add about 3 mils to the width of each column, reducing the detection area and upsetting the symmetry

even more. The background subtraction circuit is not effective unless the charge-storage capacity of the detectors is several times that of the CCD wells. In our case, the capacities are comparable, and additional capacity is available by operating the gates with two on at a time. Furthermore, our experience with the line array indicates that good uniformity is much more difficult to obtain when the charging circuit is used. Omitting the charging circuit, this array with 25 x 50 detectors will be a square 160 mils on a side, and will fit on a 250-mil chip leaving room for the peripheral structures, a line array, and test devices. There were also reasons for not including an input circuit in this device. Both the charging circuit for background subtraction and the input circuit for frame comparison are included in the *one-dimensional IR-CCD* being fabricated on the same chip. This is discussed below.

An interesting possibility is the use of this image in the time-delay-and integration (TDI) mode. In this mode, the image is mechanically scanned parallel to the "B" register columns in synchronism with the "B" register clocking. The uniformity thus obtained is that of the vidicon mode, but is improved by the effective averaging of the detector responsivities in each column. The sensitivity of the array is the same as is the storing mode. It can be viewed as having only line-storage, but with unusually large detectors.

III. THE ONE-DIMENSIONAL IR-CCD

The one-dimensional array is included on the chip to make possible experimental work on the background-subtraction mode and the frame-comparison technique. The circuits required for these functions were not included in the two-dimensional array because of the difficulties discussed above, and because it has been shown that the signal from a thermal source can be handled by the shift register without background subtraction. Indeed, the background-subtraction mode was shown to be troublesome because nonuniformities in processing get into the video signal in a fundamental way. Nevertheless, a one-dimensional array was desired for frame comparison experiments, and it is a relatively simple matter to include charging circuitry on this array. Furthermore, it gives us an opportunity to try out a new idea that may improve the uniformity of the background mode enough to make this mode feasible.

A major cause of the nonuniformity observed in the background-subtraction mode is the variation in MOS pinch-off voltage. Uniformity is good in the *vidicon* mode because a single gate (the transfer gate) is used to simultaneously charge the detectors and to read out the integrated signal. In the background-subtraction mode, as previously described and performed, two gates, the charging gate and the transfer gate perform these functions separately, and the difference between their pinch-off voltages contributes to the fixed pattern noise on the video signal. To eliminate this source of nonuniformity, we must use a single gate, the transfer gate, to establish both of the charging and the transfer levels. This can be accomplished with the circuit shown in Fig. 6. There, the charging circuit is shown on the opposite side of the shift register from the detectors. Operation of this circuit is shown in Fig. 7. Once per frame, while phase-1 gates are on, the charging gate is pulsed on, making the surface under it go to V_A. The transfer gate is simultaneously pulsed, driving its surface to V_C, establishing the charging level. The charge thus drained away can be much larger than the well capacity, since the phase-1 gates are used as transmission channels, not storage wells. After the integration time the transfer gate is pulsed to a smaller value, making the surface under it V_D. The smaller signals thus skimmed are accumulated under the phase-1 gates and clocked out in the usual manner. It is desirable

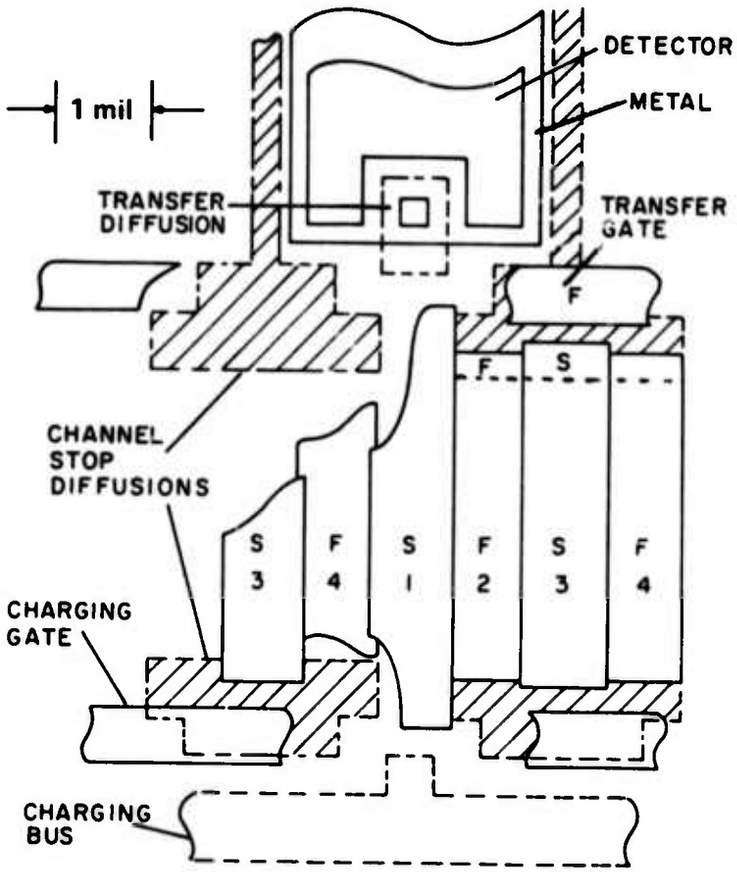

Fig. 6. Scale drawing of one stage of the 1-D line array. The gates are drawn broken to reveal the diffusions. The design is symmetrical about the phase-1 gate.

to recharge the detectors immediately after skimming so that the detectors can integrate the optical signal while the transferred scene is being read out. Recharging the detectors is obviously impossible while the signal charges are stored under the phase-1 gates, but these charges can be clocked to the phase-3 wells for temporary safekeeping while the phase-1 gates are used as transmission channels. This would be impossible in a charge-coupled shift-register with fewer than four phases.

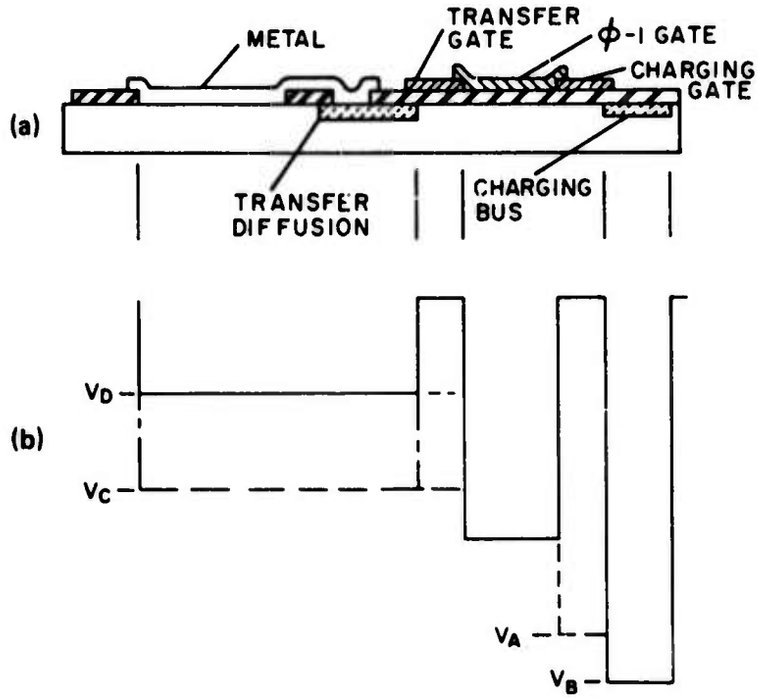

Fig. 7. (a) Cross-sectional view of one-dimensional IR CCD with new background-subtraction scheme. (b) Energy level diagram aligned with "a". Some details were omitted for clarity. The solid lines show the phase 1 gate on, and the transfer and charging gates off.

IV. QUANTITATIVE INFRARED MEASUREMENTS

A. MEASUREMENTS ON ISOLATED DETECTORS

The new chips will include test detectors that are identical to those in the array in size and contacting method, and will be isolated with channel stop diffusion. These will be bonded directly for tests that can be more conveniently made on individual detectors. These tests include dark current, dark current noise, blackbody current responsivity, and blackbody detectivity in a simulated high background.

The dark current will be measured as a function of reverse bias to establish the maximum voltage to which the detectors can be set. This measurement requires nothing more than a variable bias supply and an electrometer. The blackbody "short-circuit" current responsivity can be measured in the conventional way as shown in Fig. 8. The load resistance should be small compared with the detector resistance to guarantee short-circuit conditions and, in addition, not so large as to give excessive RC time constants with the stray capacitance. The load resistance should, however, be large enough to produce a measurable IR drop for the lock-in amplifier. Preliminary computations indicate that 5-MΩ load resistance (i.e., actual load resistance in parallel with the lock-in input impedance) will be satisfactory for a 0.5-in.-diameter 500°K blackbody positioned about 1 ft. in front of the detector and chopped no faster than 100 Hz. The blackbody current responsivity in amperes/watt will be measured as a function of bias voltage and frequency (to remove any residual RC time constant effects).

The dark current noise spectrum can be measured by modifying the circuit of Fig. 8 in the following way. The 500°K blackbody and its associated chopping wheel are removed and the detector kept in the dark. The lock-in amplifier is provided with an output that permits it to be used as a high quality preamplifier. Its output can be measured with a wave analyzer that measures the RMS noise in a small bandwidth (7 Hz) about any desired frequency. We will be interested in frequencies from about 10 Hz (the lowest measurable with this instrument) to about 100 Hz (the highest frequency one can go to without RC time constant becoming important). We will be interested in the noise spectrum from 10 to 100 Hz as a function of bias level.

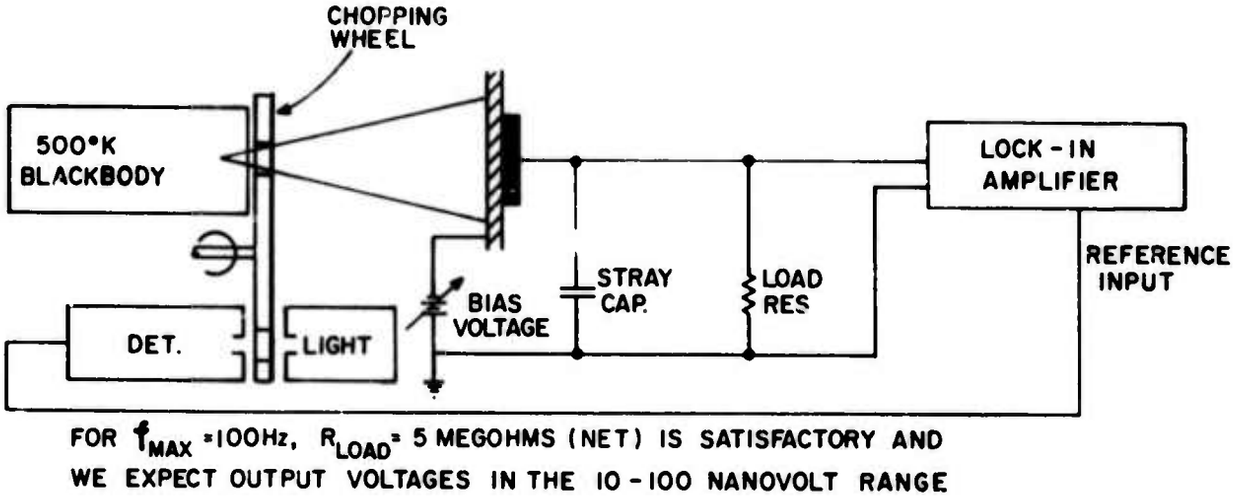

Fig. 8. Measurement of blackbody current responsivity of the isolated test detector.

The measurement of blackbody detectivity in a simulated high background is a combination of the above responsivity measurement and the noise measurement but in the presence of an artificial dc background to simulate conditions that would be encountered in the 3- to 5-μm region in thermal imaging applications. Preliminary computations indicate that the 500°K blackbody is not capable of producing this background, so that we will have to make another larger and/or hotter source (e.g., a large soldering iron viewed on end) and use the detector per se to calibrate its intensity (which becomes possible after the initial responsivity measurement above has been made). We are interested in the responsivity and noise under these high background conditions as a function of frequency and bias voltage. In this way, we can find the blackbody detectivity as a function of frequency and bias voltage in general, and the conditions for maximum detectivity in particular. BLIP conditions will be indicated by a noise level much larger than the dark value.

Since the wavelength dependences of palladium-silicide and platinum-silicide Schottky-barrier diodes on p-silicon are well known and reported in the literature, these measurements need not be repeated. It is probably sufficient to convert the measured blackbody values to the corresponding peak values and thus estimate the most important point on the spectral responsivity and detectivity curves. The detector time constant is undoubtedly very small compared with a frame time and thus not an important parameter in the

present array application. Its measurement would be difficult in view of the large stray capacitance in the proposed measurement setup and probably not worth the effort required to make a meaningful measurement.

Measurements can also be made on the isolated detectors in a storage mode to more closely simulate the vidicon mode. The diode is charged at the beginning of both the light and dark periods of the chopper cycle, and the charge pulse current is measured for each. Both dark current and responsivity can thus be measured. Measurements of this type have been made before.*

B. MEASUREMENTS ON THE ARRAYS

The pattern of dark currents over the array can be measured by simply operating the array with a long integration time in the dark and looking at the video signal which can be displayed to obtain a "picture" of the dark current variations over the array. After measuring the dark current variations for long integration times, their effects at normal integration times will be computed and evaluated.

The array can be provided with a uniform illumination from the 500°K blackbody source (no lens) and the amplitude of the video signal corresponding to each detector noted and compared with the others as a measure of uniformity. Longer than normal integration times can be used to increase the sensitivity, but not so long as to introduce appreciable dark currents. If desired, the resulting fixed pattern noise can be displayed and photographed.

The above uniformity of response measurement is, in principle, a responsivity measurement if the input light is well calibrated and dark currents are negligible. However, it is probably more convenient to chop the blackbody source and then forget about all perturbing dc effects (such as dark currents). In this case we would chop at 1/2 the frame rate (or less) and look at the change in video signal so produced at points corresponding to each of the array detectors.

The effect of background level on responsivity can be studied by just adding a dc component of input light (e.g., that hot soldering iron viewed endwise) during this measurement. The previously calibrated individual test detector could be used to measure the magnitude of the artificial background level so produced.

*F. D. Shepherd, Private communication.

The all-over system noise on the output video signal (either in the dark or under simulated high background conditions) can be measured directly with the lock-in preamplifier and wave analyzer if the read-out can be made continuous (i.e., no retrace or fly-back intervals) and the fixed pattern noise is not excessive. If the responsivity to the chopped 500°K blackbody is simultaneously measured under identical conditions, a system blackbody detectivity can be computed and directly compared to the individual test detector results.

The following tests of picture quality are planned.

(1) Cross-Talk - Image a sharp bright-dark edge on the array and examine the display for evidence of signal from the light areas getting into the dark areas. Use a circle for this test so that cross-talk in all directions will be examined.

(2) Sensitivity as a Thermal Imaging Device - Image the cold blackbody on the array so that it fills the field of view of several array elements. Then turn on the blackbody and allow it to come up to temperature and note when it can first be seen thermalwise. Note the blackbody temperature at this point and the F number of the optics.

(3) Subjective Evaluation - Image a picture and/or a test pattern on the array and look at the display and evaluate it subjectively at different illumination levels.

Image some hot objects onto the array using both reflected and self-emitted light. What, if anything, is added to the display by the sensitivity to thermal radiation from the hot object?

Some of these measurements can be made on the existing line arrays. It has been calculated* that paladium-silicide Schottky barriers should have the equivalent response for 70°C scenes that platinum-silicide barriers have for 15°C scenes. Measurements on the existing line-arrays may indicate whether we can achieve this.

When measurements are made on the platinum-silicide array, it may be possible to improve the performance of this imager by cold filtering. A 3.4- to 4.2-μM cold filter will reduce the background response of a platinum-silicide array by 40% while improving the signal-to-noise ratio.*

*F. D. Shepherd, Private communication.

V. INITIAL INFRARED MEASUREMENTS

Infrared measurements were begun using a 500°K blackbody with the existing 64 x 1 line array chips. The blackbody source had a 1/2-in. aperture, and was placed 6 in. away from the array which was under liquid nitrogen in the quartz optical dewar. The frame integration was increased to 160 ms. Under these conditions, the blackbody accounted for 30 mV of video signal. Measurements were made on the line arrays with electrical input, establishing that the floating diffusion and the gate connected to it have a combined capacitance to the substrate of 0.5 pF. Thus, the current produced by the 64 detectors was (charge on floating diffusion) x 64 x (frame rate)

$$= C_{diff} \times \Delta V_{diff} \times 64 \times (1/0.160 \text{ sec})$$

$$= 0.5 \times 10^{-12} \text{ f} \times 0.030 \text{ V} \times 64/0.16 \text{ sec} = 4.5 \times 10^{-12} \text{ A}.$$

This current was used along with knowledge of the detector areas and the output spectrum of the 500°K blackbody to quantitatively scale the spectral sensitivity curve of the detectors which was included in the previous report.[1] The result was that the maximum quantum efficiency of the detector just beyond the intrinsic silicon absorption region is 2%.

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1. E.S. Kohn, "Charge-Coupled Scanned IR Imaging Sensors," AFCRL-TR-75-0284, Semiannual Report No. 3, prepared for Air Force Cambridge Research Laboratories under Contract No. F19628-73-C-0282, 15 May 1975.

VI. CONCLUSIONS

The program for making two-dimensional images is well under way. A plan for making quantitative infrared measurements on the arrays has been devised, and tests have already begun on existing arrays.

PUBLICATIONS

A paper based on this work was presented on October 29, 1975 at the 1975 International Conference on the Application of Charge-Coupled Devices, and is published in the Proceedings of that conference on pages 59 through 69. The title and abstract follow below.

INFRARED IMAGING WITH MONOLITHIC, CCD-ADDRESSED SCHOTTKY-BARRIER DETECTOR ARRAYS: THEORETICAL AND EXPERIMENTAL RESULTS*

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and

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The theoretical basis for infrared imaging in the 3-to 5-μm spectral band with CCD addressed silicon Schottky-barrier mosaics will be presented. A unique approach is used which allows readout of majority carrier signals with depletion mode CCD's. Photo-response, contrast, and noise relationships for this type of all solid-state sensor are derived. It is seen that the use of the Schottky barrier internal-photoemission process, which is independent of lifetime or doping variations in the silicon wafer, leads to at least a factor of 100 improvement in infrared photoresponse uniformity. This advance permits for the first time the development of infrared cameras that are not limited by fixed pattern noise. Systems considerations such as cooling requirements, noise mechanisms, cutoff wavelengths, and the effects of atmosphere attenuation will be related to signal contrast, and noise-equivalent-temperature (N.E.ΔT.). Finally the operation of IR-CCD cameras will be compared to IR line scanners, so as to define the specific Schottky camera parameters that are required for equal performance.

A charge-coupled imager sensitive to infrared light as far out as 3.5 μm has been fabricated and operated. It consists of a linear array of 64 Pd:p-Si Schottky-barrier detectors adjacent to a three-phase charge-coupled shift register. The design has a single level of metallization with gaps. A single transmission gate, when pulsed on, coupled each detector to its associated shift register gate thus reverse-biasing the detectors. The charges transferred to the shift register are then read out sequentially to produce the video signal. It is demonstrated that in this mode of operation, the IR-CCD is particularly immune to non-uniformities in substrate doping and in MOSFET pinch-off voltage.

*This work was funded by the Defense Advanced Research Projects Agency.

Operation is similar to that of a vidicon. The shift register had transfer losses as low as 5×10^{-4} per transfer as measured with an electrical input. Visible images were sensed directly by illumination of the shift register through the gaps as well as through the unthinned substrate. Infrared images ($1.1\ \mu m < \lambda < 3.5\ \mu m$) were sensed by the Schottky-barrier detectors illuminated through the (transparent) substrate. The two imaging modes could be easily distinguished by their spectral sensitivities as well as by their response to changes in their separate integration times. All IR measurements were made at 77°K. Uniformity was within a few percent, and objects at 110°C could be detected.

A scheme for observing low-contrast, thermal scenes without requiring the charge-coupled shift register to carry the entire background signal has been implemented in the design of this chip. Operation in this mode was also demonstrated.